Method For Fabricating Poly Patterns

TECHNICAL FIELD

[0001] The present invention relates to the field of semiconductor devices, and more specifically, to the fabrication of polysilicon patterns in semiconductor devices.

BACKGROUND

[0002] Complementary metal oxide semiconductor (CMOS) devices, such as metal oxide semiconductor field-effect transistors (MOSFETs), are commonly used in the fabrication of ultra-large scale integrated (ULSI) devices. The continuing trend is to reduce the sizes of the devices and to lower the power consumption requirements. As a result, recent trends have been to utilize ultra-shallow junctions in CMOS devices.

[0003] For example, NMOS and PMOS transistors typically have a gate insulator and a gate poly formed on a substrate. The substrate, typically a silicon substrate, is doped on either side of the gate to form the source and drain. Electrodes connect to the gate poly, source, and drain. To keep the CMOS devices as small as possible, the CMOS devices are designed such that the source and drain regions and the insulating films are as small as possible, *i.e.*, the CMOS devices are designed with ultra-shallow junctions.

[0004] Furthermore, in many cases, pre-doping is performed to implant n-type impurities in an NMOS device or to implant p-type impurities in a PMOS device in the gate poly that forms the gate electrode. Pre-doping improves the threshold voltage and drive current characteristics, thereby further enhancing the performance of the transistor.

[0005] However, n-type pre-doping often results in undesired characteristics in the poly-gate profile. Generally, n-type pre-doping is performed by implanting n-type impurities, such as phosphorous, into the gate poly. Mask layers are applied and patterned to etch the gate. The mask layers are removed and an oxidation step is performed. The removal of the mask layer, however, frequently results in a "necking" or "footing" of the gate profile, *i.e.*, the sidewalls of the gate are not vertical, thereby causing device deviation due to inconsistent dopant penetration.

[0006] For example, FIG. 1 illustrates a wafer 100 with a gate structure formed thereon after an n-type pre-doping process has been performed. A substrate 110 has a gate insulator 112 formed thereon. A gate 114 is formed on the gate insulator 112, and an oxide layer is formed on the exposed areas of the gate 114 and the gate insulator 112. A neck 118 is formed on the upper portion of the gate 114. The neck 118 induces the n+ dopant to be driven to the n-light doped drain (NLDD) area, which induces poly-finger junction leakage.

SUMMARY OF THE INVENTION

[0007] These and other problems are generally reduced, solved or circumvented, and technical advantages are generally achieved, by embodiments of the present invention, which provides a method of fabricating poly patterns.

[0008] In one embodiment of the present invention, an oxidizing step is performed after a poly structure has been formed and before removing the mask. The oxidizing prevents the necking problem commonly formed when removing the mask, thereby decreasing the finger-junction leakage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0010] FIG 1 is a cross-section view of a wafer illustrating a structure having a necking profile;

[0011] FIGS. 2a-2e are cross-section views of a wafer illustrating a process of forming polysilicon structures in accordance with one method embodiment of the present invention; and

[0012] FIG. 3 is a cross-section view of a transistor fabricated in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0013] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. In particular, the method of the present invention is described in the context of forming a gate of a transistor. One of ordinary skill in the art, however, will appreciate that the process described herein may be used for forming any type of device or structure that utilizes n-type pre-doped polysilicon structures. Accordingly, the specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0014] FIGS. 2*a*- 2*e* illustrate cross-section views of a portion of a semiconductor wafer during various steps of a first method embodiment of the present invention. The process begins in FIG. 2*a*, wherein a semiconductor wafer 200 having a substrate 210 with a gate insulator layer 212 and a gate layer 214 formed thereon. The substrate 210 may be other semiconductors: silicon, glass, GaAs, silicon-on-insulator (SOI), or the like, but preferably silicon.

[0015] The gate insulator layer 212, which prevents electron depletion, is preferably an oxide layer formed by any oxidation process, such as wet or dry thermal oxidation in

an ambient comprising an oxide, H_2O, NO, or a combination thereof, or by chemical vapor deposition (CVD) techniques using is tetra-ethyl-ortho-silicate (TEOS) and oxygen as a precursor. In the preferred embodiment, however, the gate insulator layer 212 is silicon dioxide material formed by wet or dry oxidation process, such as a furnace oxidation in an ambient environment of O_2, H_2O, a combination thereof, or the like, or an in-situ steam generation (ISSG) process in an ambient environment of O_2, H_2O, NO, a combination thereof, or the like. In the preferred embodiment, the gate insulator layer is about 15 Å to about 25 Å, but most preferably about 20 Å in thickness.

[0016] The gate layer 214 is generally a semiconductor material such as polysilicon, amorphous silicon, or the like. In the preferred embodiment, polysilicon is deposited undoped by low-pressure chemical vapor deposition (LPCVD) to a thickness in the range of about 2500 Å to about 1500 Å, but most preferably about 1800 Å.

[0017] In the preferred embodiment in which the gate layer 214 comprises a polysilicon material, the polysilicon is pre-doped with phosphorous ions at a dose of about $3.0e^{15}$ to about $6.0e^{15}$ atoms/cm^2 and at an energy of about 10 to about 30 KeV. Alternatively, the gate layer 214 may be pre-doped using nitrogen, arsenic, antimony, or the like.

[0018] Optionally, the gate layer 214 may be patterned prior to pre-doping to restrict ion implantation to pre-determined areas of the gate layer 214. For example, if multiple devices are being formed that require varying levels of doping or varying types of doping (*e.g.*, N-type doping, P-type doping, no doping, and the like), a mask layer (not shown) may be utilized to selectively dope the gate layer 214.

[0019] FIG. 2*b* illustrates the wafer 200 after a mask layer 213 has been applied in accordance with an embodiment of the present invention. The mask layer 213 protects the underlying gate layer 214 during subsequent processing steps, such as etching, to form the desired structures. In the preferred embodiment, the mask layer 213 comprises a plasma-enhanced oxide (PEOX) layer 216 and a silicon oxynitride (SION) layer 218, but other mask layers may be used, such as photoresist, TEOS oxide, or the like. The PEOX layer 216 is preferably about 200 Å to about 300 Å in thickness, but most preferably about 260 Å in thickness. The SION layer 218 is preferably about 100 Å to about 200 Å in thickness, but most preferably is about 150 Å in thickness. The PEOX layer 216 and the SION layer 218 may be deposited by any suitable method known in the art such as CVD-Nitride.

[0020] FIG. 2*c* illustrates wafer 200 of FIG. 2b after the gate insulator layer 212 and gate layer 214 have been etched in accordance with one embodiment of the present

invention. In the preferred embodiment, the gate insulator layer 212 and gate layer 214 are patterned and etched to form a gate structure 220. To pattern the gate insulator layer 212 and gate layer 214, a patterned mask (not shown), such as a photoresist mask, may be formed on the mask layer 213. In the situation wherein a photoresist process is used, a photoresist material is deposited on the SION layer 218, exposed in accordance with a mask, and developed to remove the unwanted areas of the photoresist material.

[0021] After the SION layer 218 and PEOX layer 216 have been patterned, the wafer is etched to remove unwanted portions of the gate insulator layer 212, gate layer 214, PEOX layer 216, and SION layer 218. The etching process may be a wet or dry, anisotropic or isotropic, etch process, but preferably is an anisotropic dry etch process.

[0022] FIG. 2*d* illustrates wafer 200 of FIG. 2*c* after an oxidation step has been performed in accordance with an embodiment of the present invention. The oxidized regions 222 are generally formed on the substrate 210 and along the sidewalls of gate structure 220. The oxidized regions 222 form a protective barrier layer on top of the substrate 210 and along the sidewalls of the gate structure 220 during succeeding steps.

[0023] Oxidation may be performed by any oxidation process, such as wet or dry thermal oxidation. Preferably, however, a dry oxidation step, such as a furnace anneal, a rapid thermal oxidation (RTO), or the like, is performed. Most preferably, an RTO

process is performed at a temperature of about 900° to 1010° C with an ambient comprising an oxide, O_2 a combination thereof, or the like, for a duration of about 5 seconds to about 15 seconds. The oxidized region 222 is preferably about 15 Å to about 25 Å in thickness.

[0024] FIG. 2*e* illustrates wafer 200 of FIG. 2*c* after the mask layer 213 has been removed in accordance with an embodiment of the present invention. In the preferred embodiment wherein the mask layer 213 comprises a PEOX layer 216 and a SION layer 218, the mask layer 213 is preferably removed by performing a wet dip in phosphoric acid (H_3PO_4) for about 8 minutes to about 12 minutes, but most preferably about 10 minutes. The removal of the mask layer 213 may cause the oxidation layer 222 along the side of the gate structure 220 and the substrate 210 to be partially or entirely removed. The sidewalls of the gate structure 220 should remain substantially vertical after the removal of the mask layer 213, providing a better finger-junction profile and reduced poly finger junction leakage.

[0025] Thereafter, standard processing steps such as doping, oxidation, etching, layering, and the like, may be performed to fabricate semiconductor devices, such as transistors.

[0026] FIG. 3 illustrates a transistor 300 that may be formed in accordance with one embodiment of the present invention discussed above with reference to FIGS. 2*a*-2*e*, wherein like reference numerals refer to like elements. In this case, the gate insulator layer 212 and gate layer 214, collectively referred to as a gate 308, form a gate of a transistor. The substrate 210 contains doped areas 310 (source/drain) that represent the source and drain of the transistor 300. The insulator regions 312 along the sidewalls of the gate 308 provide spacers for the gate 308.

[0027] Although particular embodiments of the invention have been described in detail, it is understood that the invention is not limited correspondingly in scope, but includes all changes, modifications, and equivalents coming within the spirit and terms of the claims appended hereto. For example, differing types of mask materials and photoresist materials may be used, varying thicknesses of the gate layer, gate insulator layer, and, mask layer, may be used, and the like. Accordingly, it is understood that this invention may be extended to other structures and materials, and thus, the specification and figures are to be regarded in an illustrative rather than a restrictive sense.